ABSTRACT

[0040] A method of fabricating an on-chip decoupling capacitor which helps prevent L di/dt voltage droop on the power grid for high surge current conditions is disclosed. Inclusion of the decoupling capacitor on die directly between the power grid greatly reduces the inductance L, and provides decoupling to reduce the highest possible frequency noise. This invention specifically describes the process flow in which the decoupling capacitor is located between the top layer metallization and the standard bump contacts which have either multiple openings or bar geometries to provide both power grid and top decoupling capacitor electrode contacts.